REMARKS

Applicants note that new claims 44-59 were added in the previous Response. No new matter was added. Support for the new claims is found in at least Figure 3 and the associated discussion in the present application. Independent claims 1 and 47 have been amended and claims 5 and 51 have been canceled. Thus, claims 1-4, 6-12, and 44-50 and 52-59 are pending in the present application.

In the Office Action, claims 1-2, 4-8, and 10-12 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Yoshimura, et al (U.S. Patent Application Publication No. 2004/0135226). Claim 3 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yoshimura in view of Ridinger (U.S. Patent No. 4,724,219). Claim 9 was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yoshimura in view of Jang (U.S. Patent No. 6,049,137). The Examiner's rejections are respectfully traversed.

With regard to amended independent claim 1, Applicants describe and claim providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting layer positioned above the insulating layer. For example, Applicants describe forming a silicon-on-insulator (SOI) structure including a silicon substrate, a silicon dioxide insulating layer, and an epitaxial silicon semiconductor layer. See Patent Application, page 10, ll. 21-24 and Figure 1. Applicants further describe and claim forming an opening in the semiconducting layer and the insulating layer to thereby expose a surface area of the bulk substrate. Applicants also describe and claim forming a patterned layer of photoresist above the exposed surface area of the bulk substrate and performing at least one etching process to form an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate using

the patterned layer of photoresist as a mask for the at least one etching process. Applicants then describe and claim forming a layer of material above the alignment mark and in the opening.

Yoshimura describes a silicon-on-insulator substrate 20 that includes a silicon support substrate 21A on which a silicon dioxide buried insulating layer 21B is formed. An active layer 21C of single crystal silicon is then formed on the silicon dioxide buried insulation layer 21B. An opening 24A is formed in an alignment mark formation region 20B and a silicon nitride film 23 is deposited over the structure. A resist pattern 25 is formed on the silicon nitride film 23 and is used to pattern the silicon nitride film 23 in the opening 24A. The resist pattern 25 is removed and the silicon nitride film 23 is used as a mask to etch grooves 21c and 21d in the silicon support substrate 21A. See Yoshimura, paragraphs [0062-0065]. Yoshimura does not, however, teach or suggest performing at least one etching process to form an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate using the patterned layer of photoresist as a mask for the at least one etching process, as set forth in independent claim 1.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Yoshimura and request that the Examiner's rejections of claims 1-2, 4-8, and 10-12 under 35 U.S.C. 102(e) be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of Yoshimura, Ridinger, or Jang, either alone or in combination. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed in detail above, Yoshimura fails to teach or suggest performing at least one etching process to form an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate using the patterned layer of photoresist as a mask for the at least one etching process, as set forth

in independent claim 1. Thus, Yoshimura fails to teach or suggest all the limitations set forth in independent claim 1.

Yoshimura also fails to provide any suggestion or motivation to modify the prior art of record to arrive at Applicants claimed invention. To the contrary, Yoshimura teaches away from the present invention. In particular, Yoshimura teaches that the silicon nitride layer 23 should be used as a mask in the device formation region 20A and the alignment mark formation region 20B so that the dry etching process used in the device formation region 20A stops upon exposure to the buried insulation layer 21B whereas etching of the grooves 21*cd* penetrates deeply into the support substrate 21A. Applicants respectfully submit that teaching use of the silicon nitride layer 23 teaches away from the use of a photoresist as a mask for forming alignment marks in the bulk substrate. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine,* 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

With particular regard to claim 3, the Examiner relies on Ridinger to teach a wafer diameter in a range of 3 to 6 inches. However, Ridinger does not remedy the aforementioned deficiencies of the primary reference. Thus, Applicants respectfully submit that claim 3 is not obvious over Yoshimura in view of Ridinger and request that the Examiner's rejection of claim 3 be withdrawn.

With particular regard to claim 9, the Examiner relies on Jang to teach positioning a wafer in a photolithography stepper tool and reflecting light off and alignment mark. However, Jang does not remedy the aforementioned deficiencies of the primary reference. Thus, Applicants

respectfully submit that claim 9 is not obvious over Yoshimura in view of Jang and request that the Examiner's rejection of claim 9 be withdrawn.

With regard to claims 44-50 and 52-59, Applicants respectfully submit that claims 44-46 depend from independent claim 1 and are therefore are allowable over the cited prior art for at least the aforementioned reasons. With particular regard to new independent claim 47, Applicants describe and claim, among other things, performing at least one etching process to form an alignment mark in the bulk substrate within an exposed unpatterned surface area of the bulk substrate using the patterned layer of photoresist as a mask for the at least one etching process. Thus, for at least the aforementioned reasons, Applicants respectfully submit that claims 47-50 and 52-59 are allowable over the cited prior art.

For at least the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: November 7, 2006

/Mark W. Sincell, Ph.D./
Mark W. Sincell, Ph.D.
Reg. No. 52,226

AGENT FOR APPLICANTS

Williams Morgan & Amerson, P.C.
10333 Richmond Avenue, Suite 1100
Houston, TX 77042
(713) 934-4052 ph
(713) 934-7011 fx